Customer No.: 31561
Application No.: 10/708,355
Docket No.: 12222-US-PA

REMARKS

Present Status of the Application

Claims 1-2 and 4-16 are still pending. Applicant respectfully traverses the Examiner's rejections based on the following arguments. Accordingly, reconsideration of this application is respectfully requested.

Discussion for rejections to claims under 35 U.S.C. 102(e)

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Chou et al (US Publication No. 2005/0055481)

In response thereto, applicant respectfully traverses the preceding objections based on the following arguments. To establish a prima facie case of anticipation, the cited reference (i.e. Chou) should teach, suggest or disclose all limitations of the claim 1. The Examiner alleged that "a silicon storage device connector, electrically coupled to the silicon storage device;" [with respect to this limitation, Chou discloses "The flash drive/reader of Figs. 1, 2 can be connected to USB link 128 of the PC]. In other words, the Examiner alleged that the flash drive/reader of Figs. 1, 2 is identical to "a silicon storage device connector," as claimed in the claim 1. However, the preceding Examiner's allegation is incorrect because obviously, "a silicon storage device connector," as claimed in the claim 1, is

a connector and thus totally different from a **flash drive/reader** as disclosed in Chou. Furthermore, the Examiner alleged that "a bridge controller, electrically coupled to the silicon storage device connector, wherein when the bridge controller receives a read instruction, the bridge controller prefetches a part of data..." [Chou discloses this limitation as "prefetching of flash data may be performed by flash-memory controller 30 (Figs. 4, 6)]. In accordance with the preceding Examiner's allegation, as "the silicon storage device connector," as claimed in the claim 1, is alleged to be identical to the flash drive/reader 65 in Fig. 4, actually, in Fig.4, the bridge controller 30 is comprised in the silicon storage device connector (or flash drive/reader 65), rather than electrically coupled to the silicon storage device connector as claimed in the claim 1.

Accordingly, Chou fails to disclose, teach or suggest "a silicon storage device connector, electrically coupled to the silicon storage device," as claimed in the claim 1. In other words, the amended claim 1 is not anticipated by Chou and thus patentable.

Discussion for rejections to claims under 35 U.S.C. 103 (a)

5. Claims 2 and 4-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Wurzburg (US 2005/0097263) in view of Chou (US 2005/0055481).

Applicant respectfully traverses the above rejections as follows. To establish a prima facie case of obviousness, all the cited references (here referred to Wurzburg

and Chou) must teach, suggest or disclose all limitations of the independent claims 2, 5 and 11.

In re claim 2, the Examiner alleged that "an allocation table buffer, electrically coupled to said system interface and said silicon storage device interface for storing a data accessing address mapping table"[Wurzburg discloses this concept in "Fig.2 illustrates a schematic diagram of one embodiment of IDE-CRs" including "an ATA command/status register emulation buffer (CSRB) 106" which equivalent to an allocation table buffer as it "translates the IDE/ATA command/status information into control and status information of a format used by a flash-memory card.]. In other words, the Examiner alleged that the CSRB 106 as disclosed in Wurzburg is identical to the allocation table buffer as claimed in the claim 2. It is noted that the Examiner uses indefinite words, "**equivalent** to" and" Wurzburg discloses this **concept**," (emphases added) which means the CSRB 106 as disclosed in Wurzburg is not absolutely identical to the allocation table buffer as claimed in the claim 2. Actually these two buffers are totally different from each other based on the following reasons:

(a) Although CSRB 106 as disclosed in Wurzburg and the allocation table buffer as claimed in the claim 2, are buffers, their achieved functionalities are totally different because of the implementation of the total different contexts contained in these two buffers. From the 9th-11th lines in paragraph [0021] in

Wurzburg, there discloses "CSRB 106, storing IDE/ATA command/status information that is used by microprocessor 108," which means CSRB 106 stores instructions such as command, rather than storing a data accessing address mapping table through the allocation table buffer as claimed in the claim 2. That is, Wurzburg is able to provide the microprocessor 108 with command/status information, whereas, the claim 2 of the present invention allows the card reader quickly access external data and stores them into the memory contained in the card reader in accordance with this data accessing address mapping table.

(b) Due to the Examiner's broadly interpreting the claim language, in paragraph [0021] in Wurzburg, the Examiner alleged that the disclosure of"An address and data bus 160 may couple CSRB 106 and MP 108, enabling data transfer between MP 108, CSRB 106 and flash media controller (FMC) 110...," discloses the relationship of **"data accessing address mapping"** in the data accessing address mapping table. However, in fact, no any technique or means regarding **"data accessing address mapping"** can be found in Wurzburg.

(c) The Examiner alleged that in paragraph [0010] in Wurzburg, there discloses "flash memory card are formatted in a Window file format such as File

Allocation Table (FTA)," so that the allocation table buffer as claimed in the claim 2 is conventional. However, the FTA format is only a format, not a buffer even it contains such a format. Thus, the allocation table buffer as claimed in the claim 2 is not disclosed in paragraph [0010] in Wurzburg.

In short, even if Chou and Wurzburg could be combined, this proposal combination still fail to teach, suggest or disclose "an allocation table buffer, electrically coupled to said system interface and said silicon storage device interface for storing a data accessing address mapping table," as claimed in the claim 2. Namely, the claim 2 is not rendered obvious by the combination of Chou and Wurzburg, and thus patentable. Thus, the claim 2 is not rendered obvious by the combination of Wurzburg and Chou and accordingly patentable.

In re independent claims 5 and 11, likewise, by the same arguments applied to the claim 2, even if Chou and Wurzburg could be combined, this proposal combination still fail to teach, suggest or disclose "card reader comprises an allocation table buffer, and the receipt of the first data is performed through a data accessing address mapping table stored in the allocation table buffer," as claimed in the claims 5 and 11. Therefore, the claims 5 and 11 are not rendered obvious by the combination of Wurzburg and Chou and accordingly patentable.

With respect to dependent claims 4, 6-10 and 12-16, they should be patentable as a matter of law for the reason that they contain all limitations of their respective patentable base claims 2, 5 and 11.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-2 and 4-16 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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Belinda Lee

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw